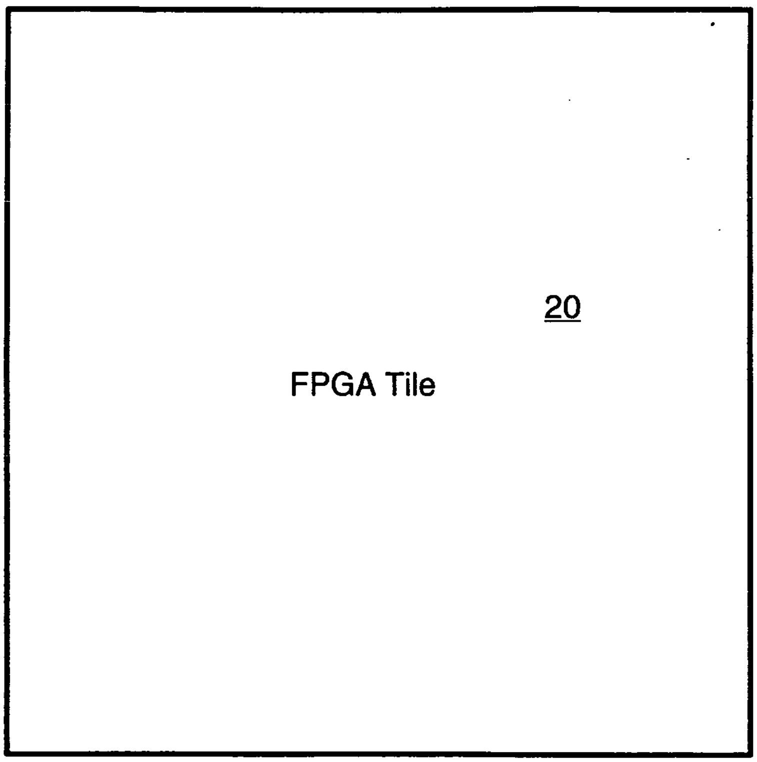

FIG. 1

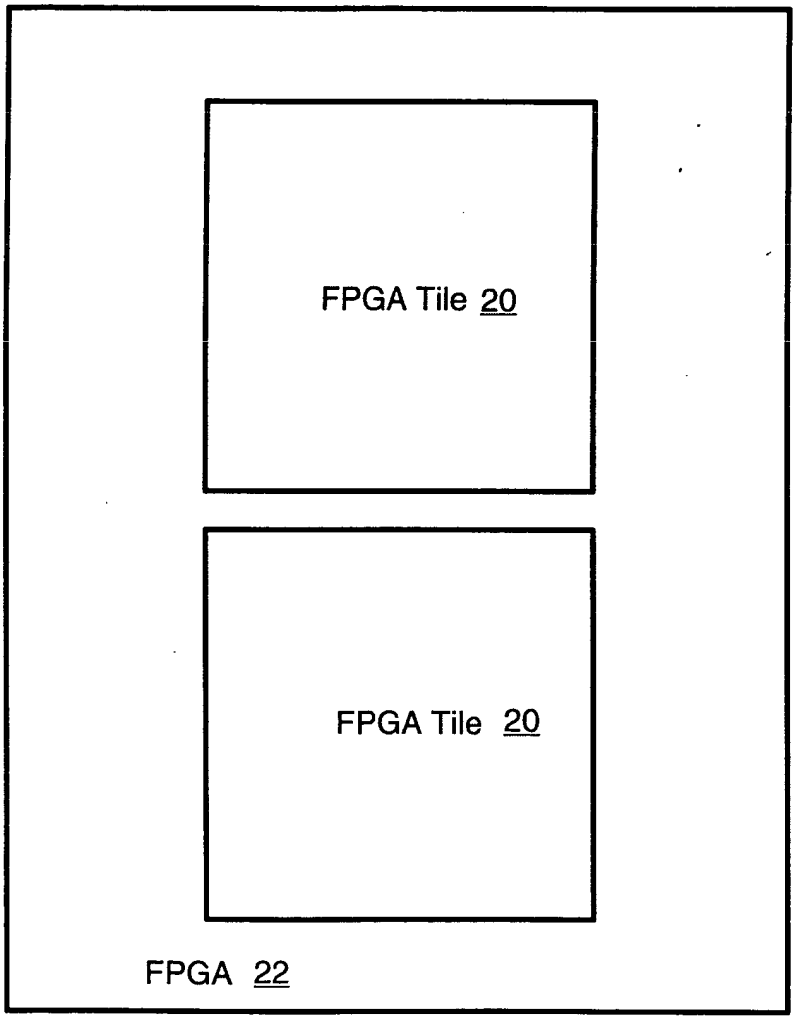

FIG. 2

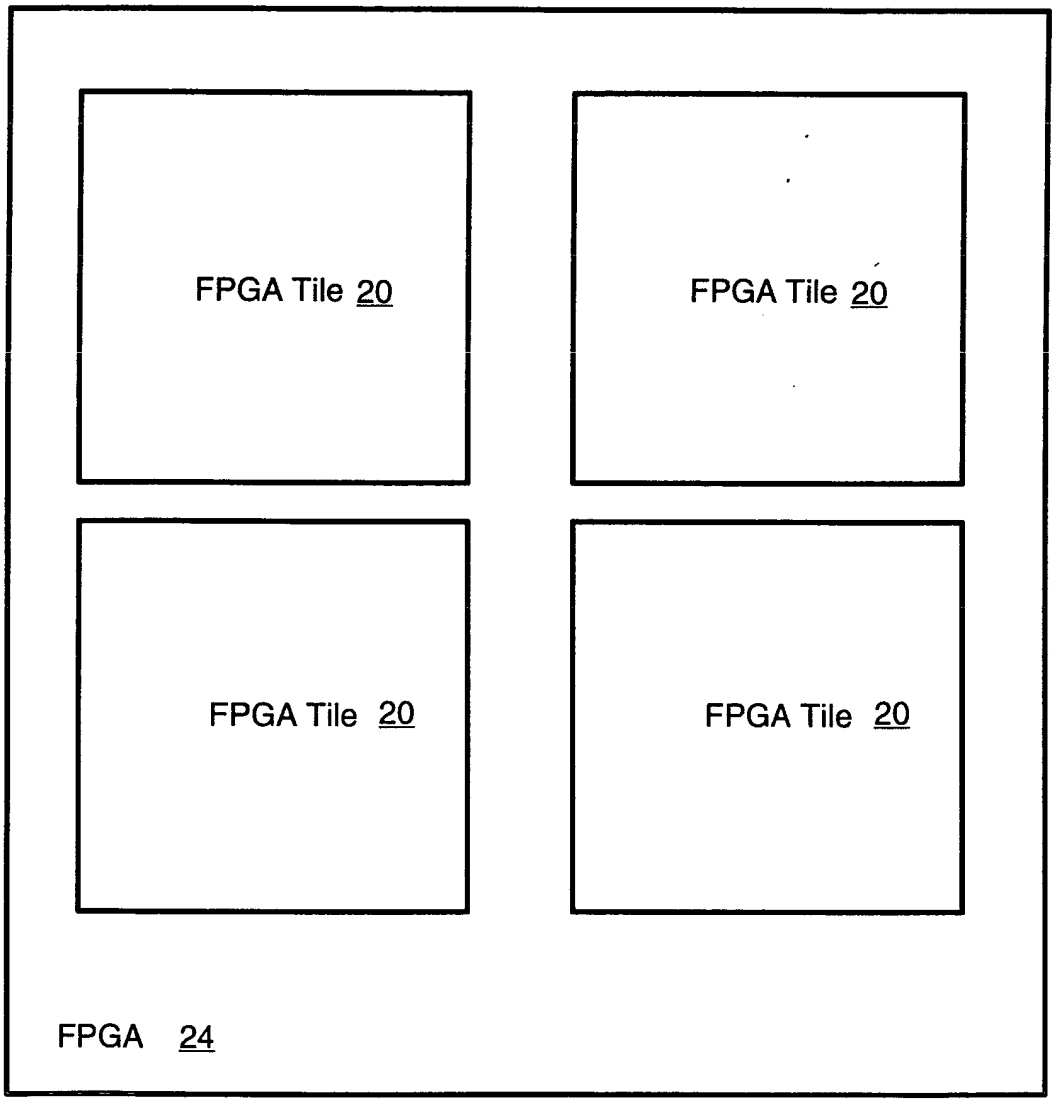

FIG. 3A

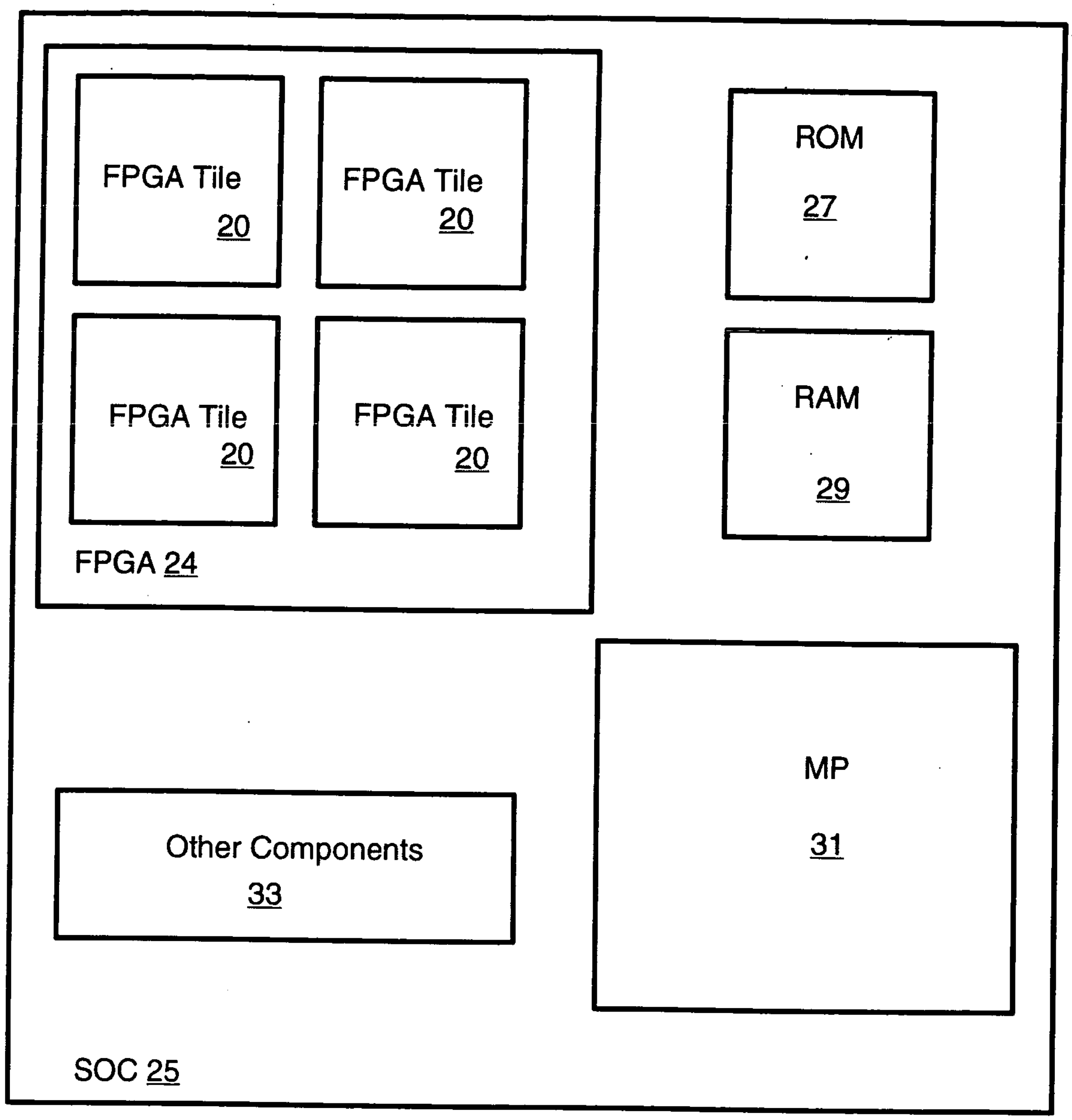

FIG. 3B

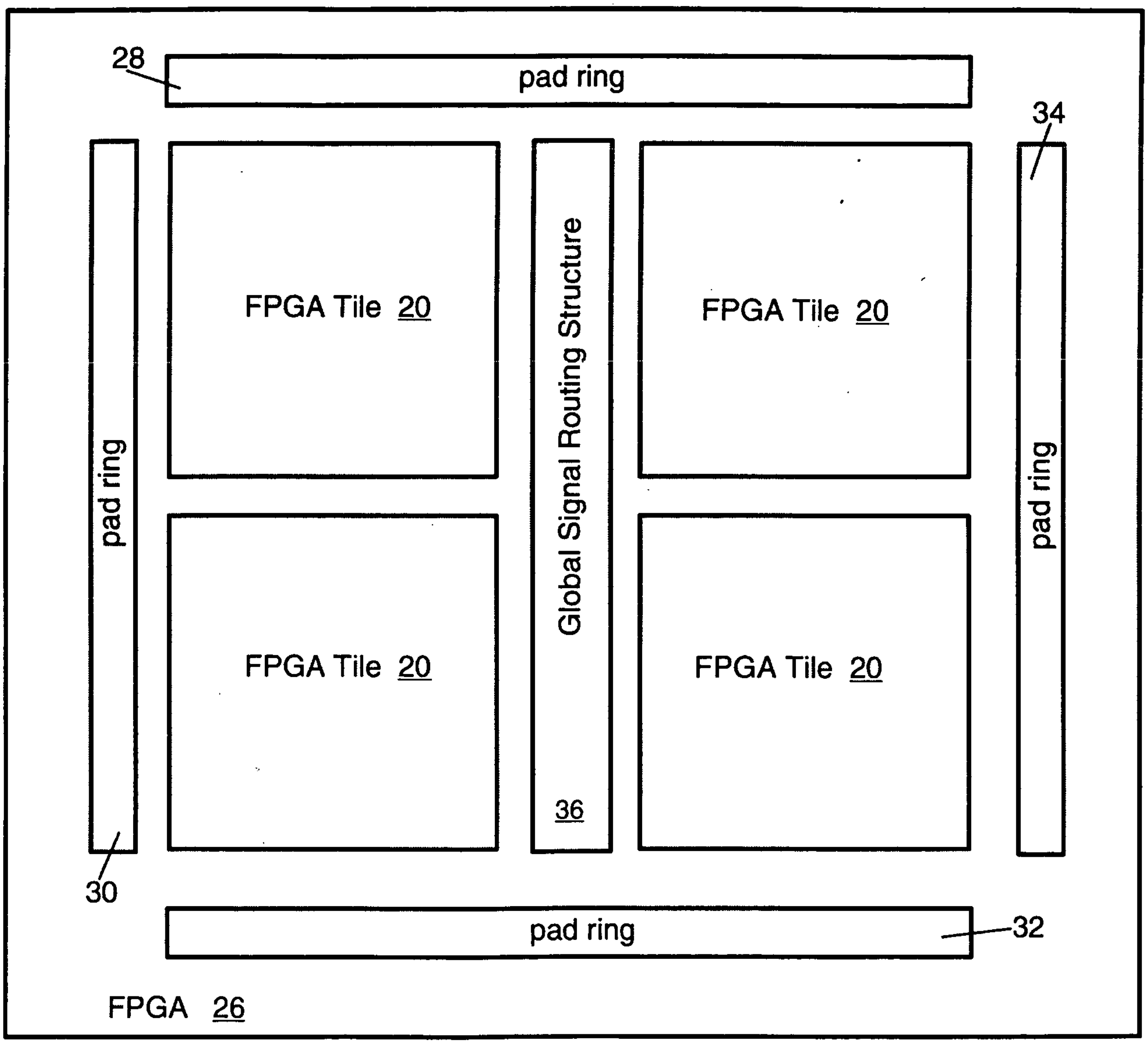
28
pad ring
34
pad ring
FPGA Tile 20
Global Signal Routing Structure
FPGA Tile 20
pad ring
FPGA Tile 20
FPGA Tile 20
36
30
pad ring
32
FPGA 26

FIG. 4

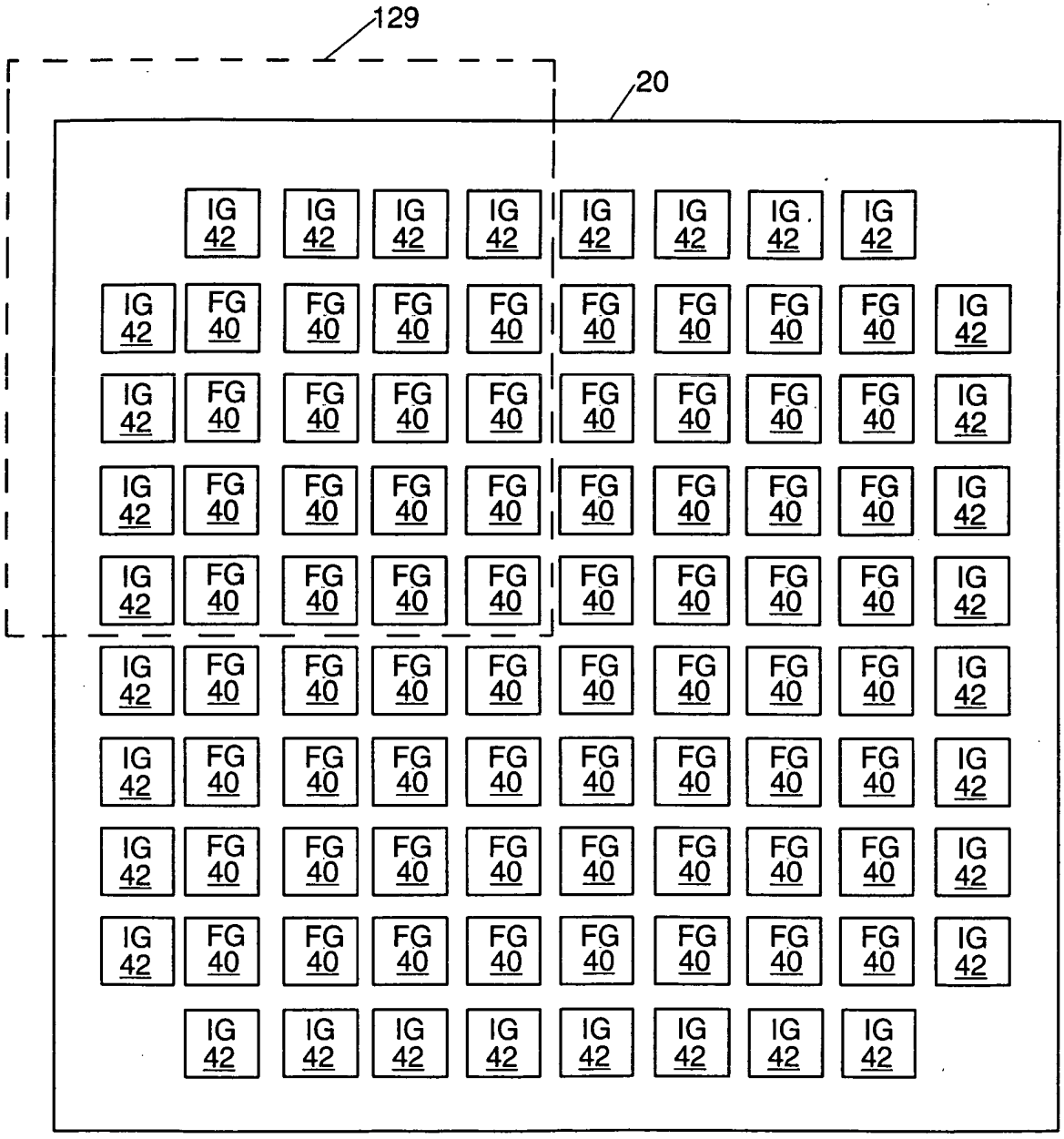

FIG. 5

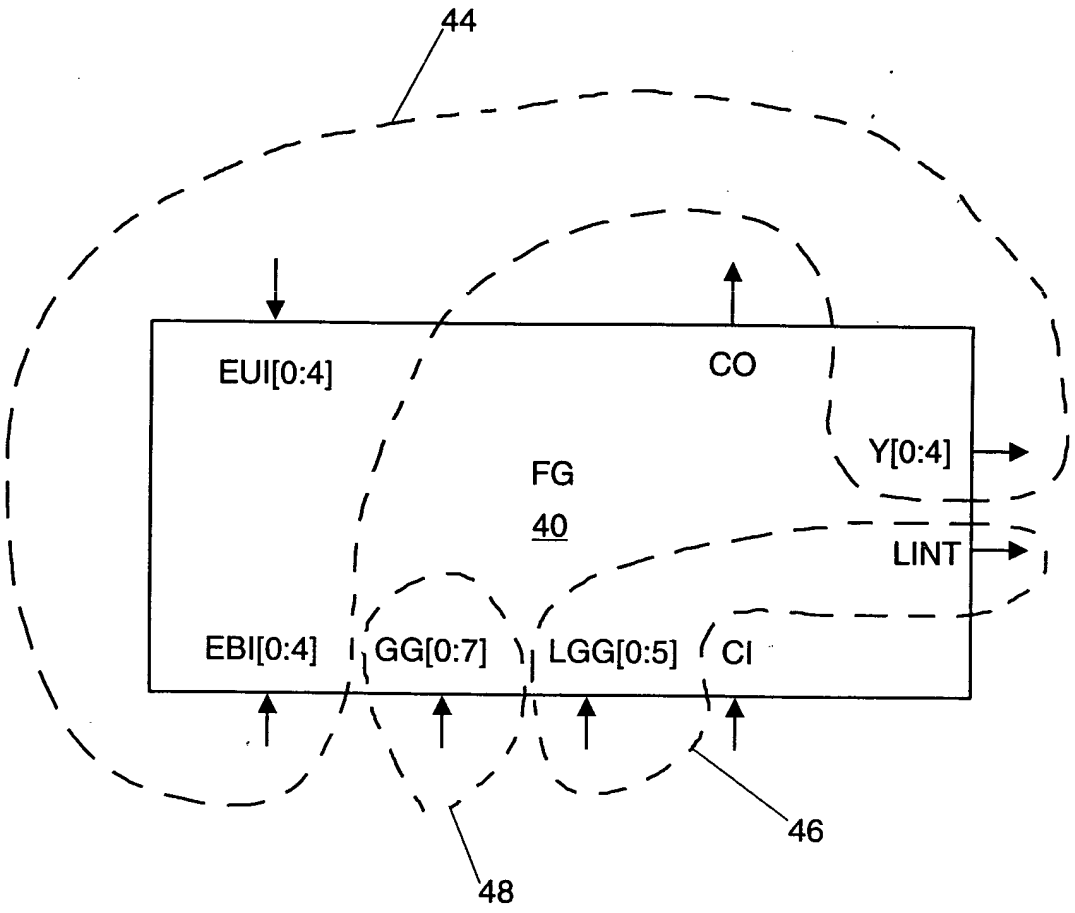

FIG. 6

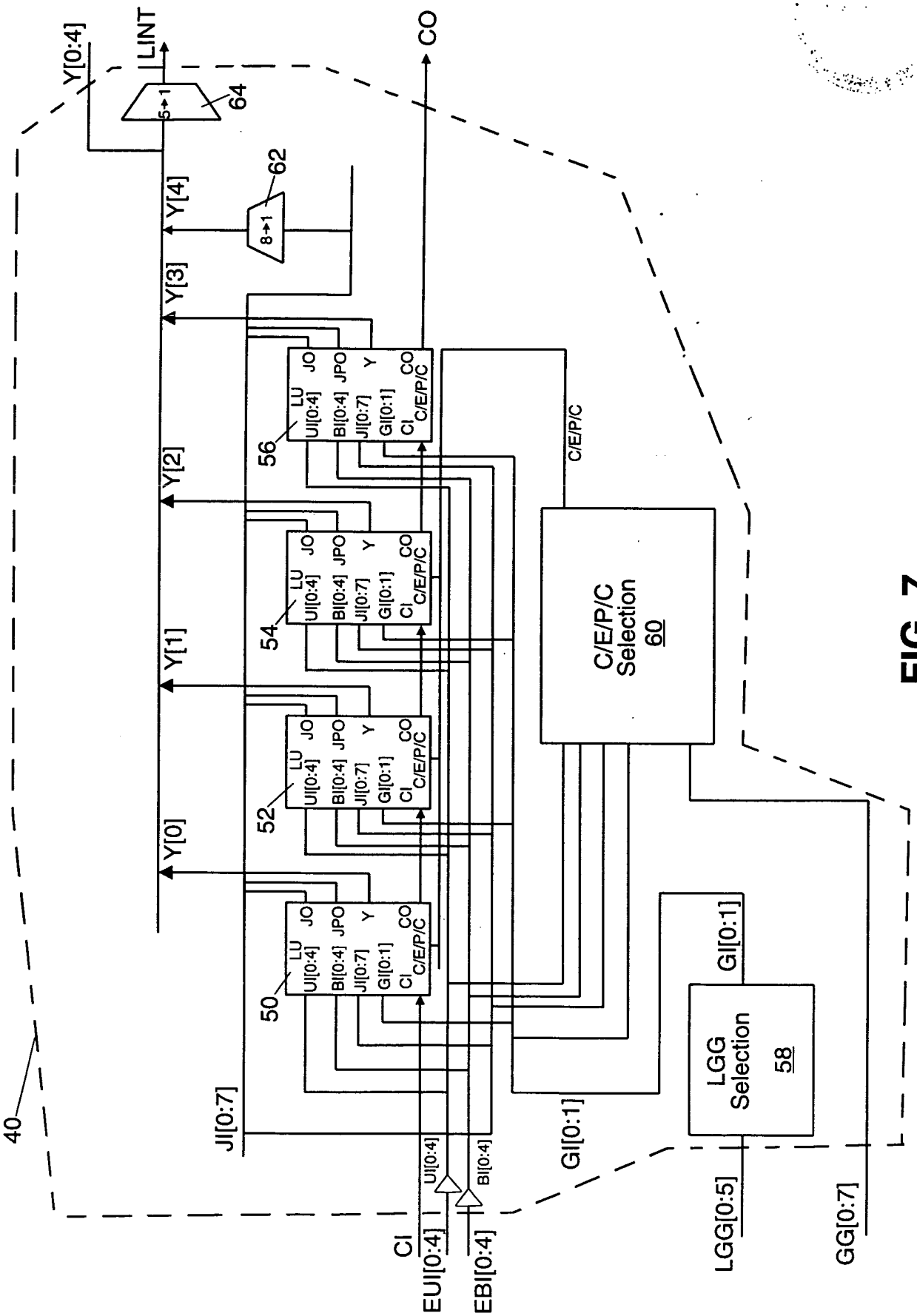
Y[0:4]
LINT
5→1
64
CO
62
8→1
Y[4]
Y[3]
Y[2]
Y[1]
Y[0]
56
54
52
50
LU
JO
JPO
Y
CO
UI[0:4]
BI[0:4]
JI[0:7]
GI[0:1]
CI
C/E/P/C
C/E/P/C
C/E/P/C Selection
60
LGG Selection
58
GI[0:1]
JI[0:7]
GI[0:1]
UI[0:4]
BI[0:4]
CI
EUI[0:4]
EBI[0:4]
LGG[0:5]
GG[0:7]
40

FIG. 7

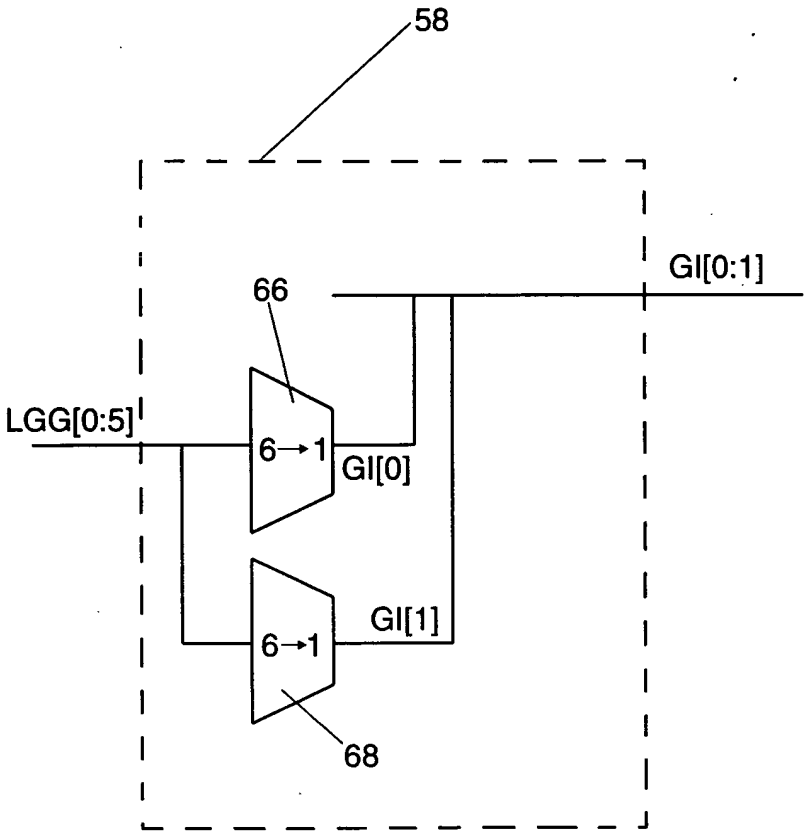

FIG. 8

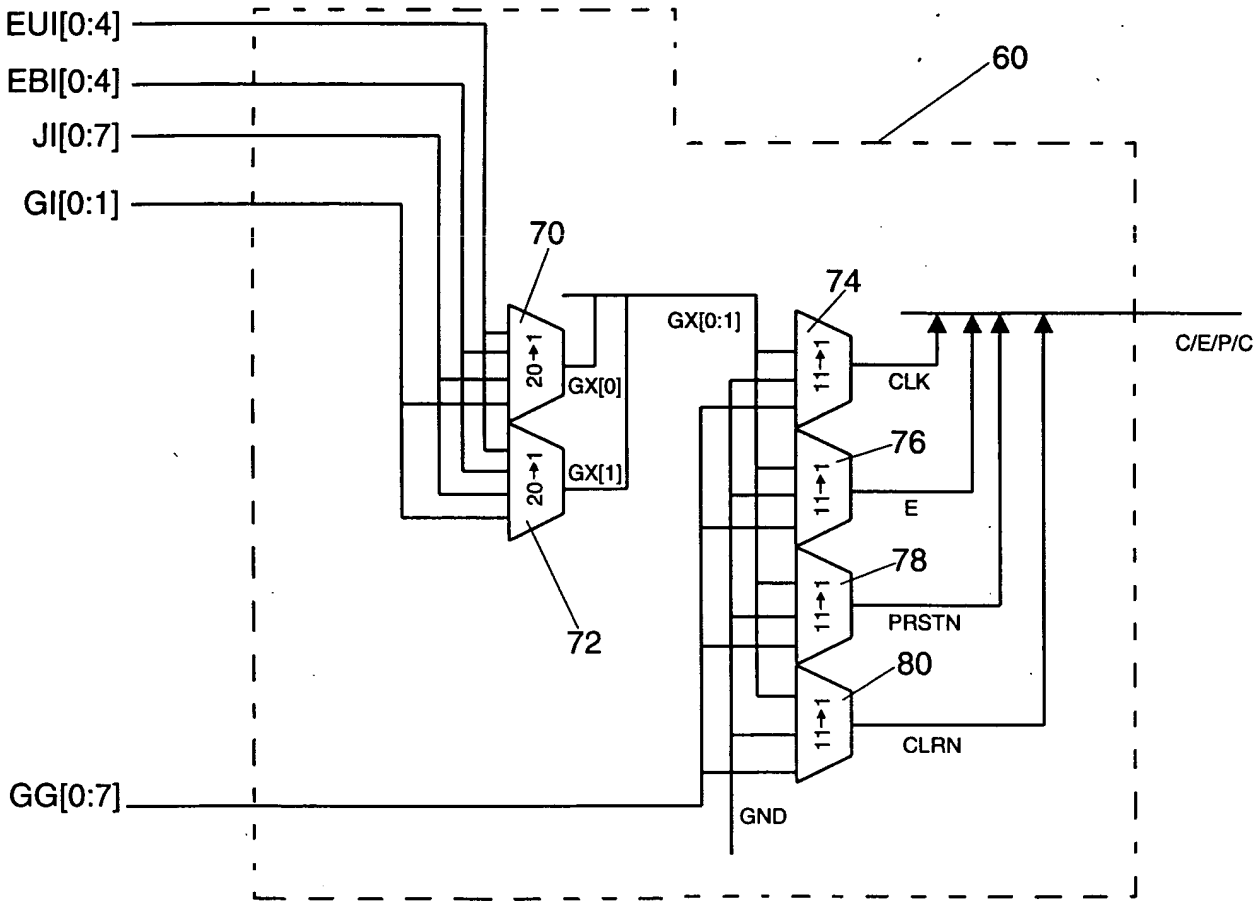
EUI[0:4]
EBI[0:4]
JI[0:7]
GI[0:1]
GG[0:7]
60
70
72
74
76
78
80
20→1
20→1
GX[0]
GX[1]
GX[0:1]
11→1
11→1
11→1
11→1
CLK
E
PRSTN
CLRN
GND
C/E/P/C

FIG. 9

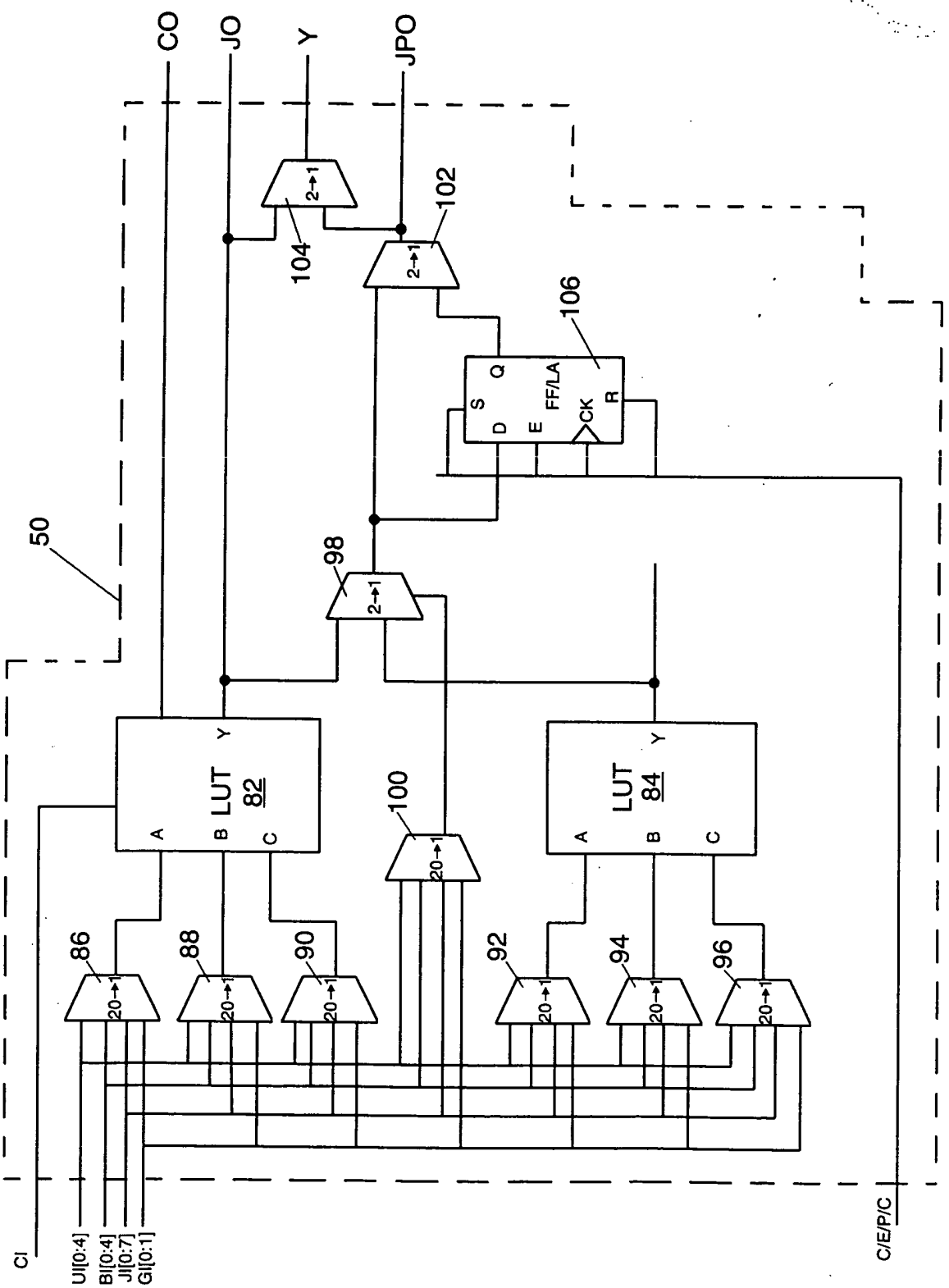
CO
JO
Y
JPO
50
102
104
106
98
100
LUT 82
LUT 84
A
B
C
Y
S
Q
D
E
FF/LA
CK
R
2→1
20→1
86
88
90
92
94
96
CI
UI[0:4]
BI[0:4]
JI[0:7]
GI[0:1]
C/E/P/C

FIG. 10

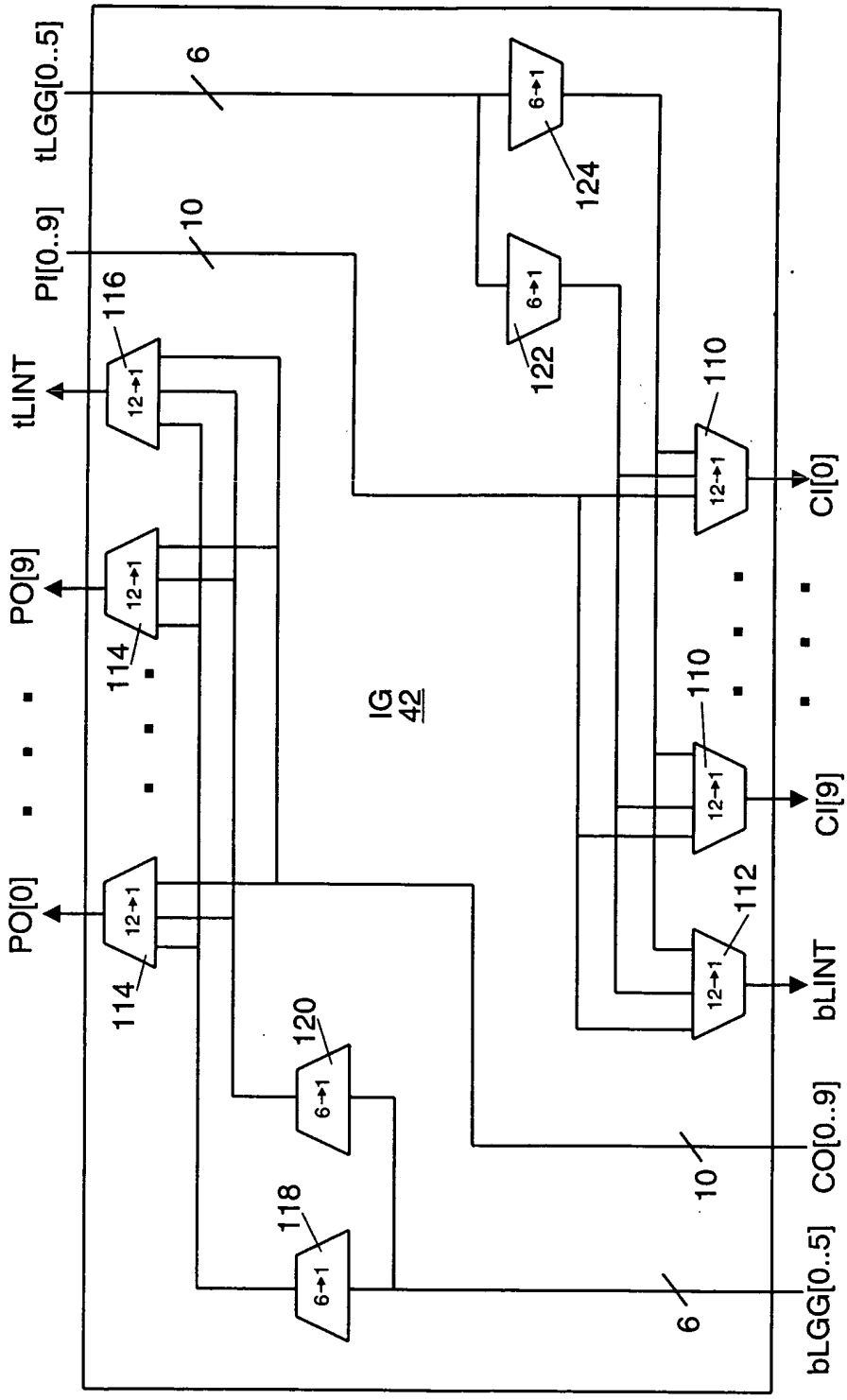
tLGG[0..5]
6
PI[0..9]
10
tLINT
PO[9]
PO[0]
IG
42
CI[0]
CI[9]
bLINT
CO[0..9]
bLGG[0..5]
12→1
6→1
110
112
114
116
118
120
122
124

FIG. 11

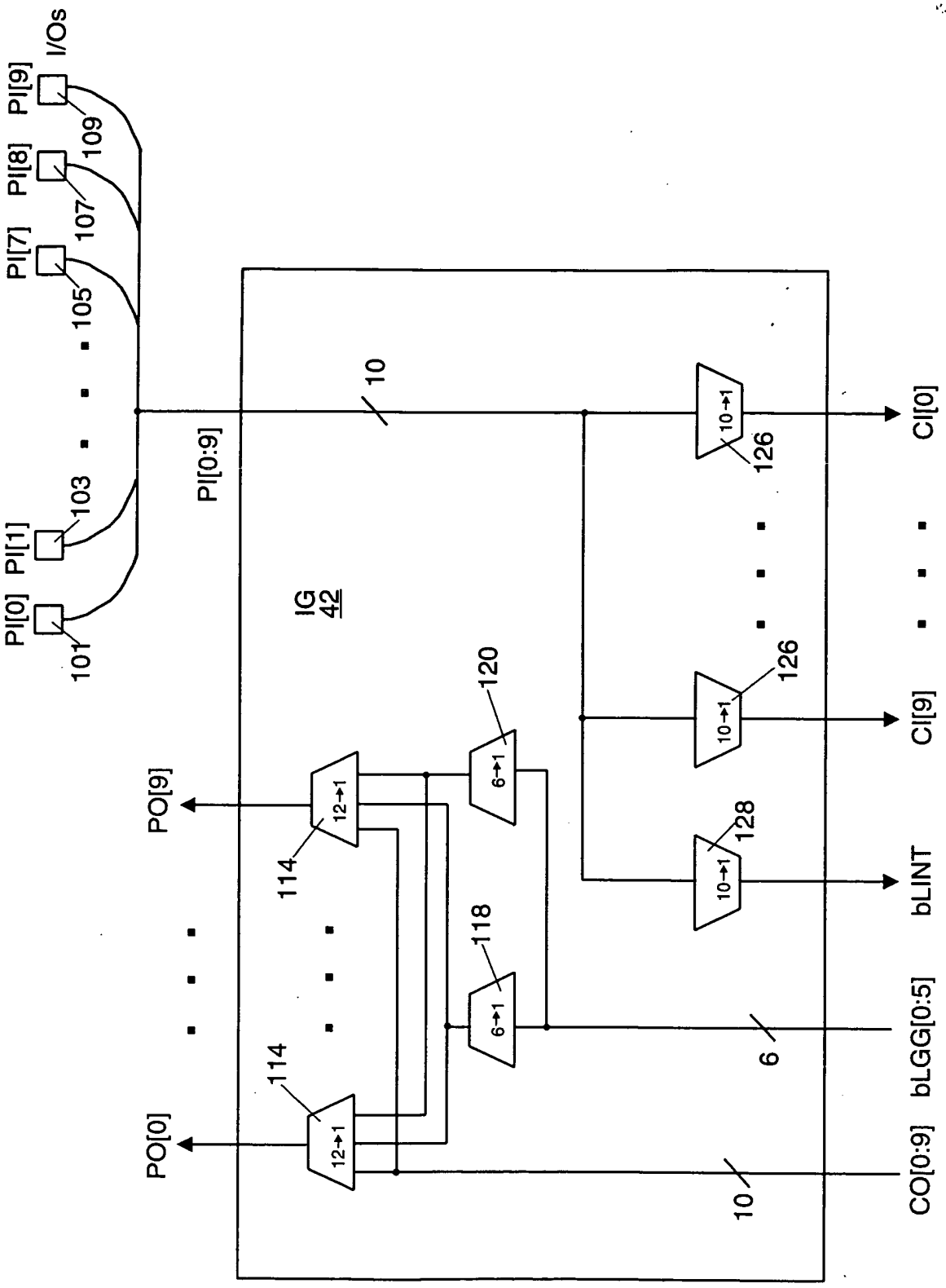
I/Os
PI[9]
PI[8]
PI[7]
PI[1]
PI[0]
109
107
105
103
101
PI[0:9]
10
IG
42
PO[9]
PO[0]
114
114
12→1
12→1
120
6→1
118
6→1
10→1
126
10→1
126
10→1
128
CI[0]
CI[9]
bLINT
bLGG[0:5]
CO[0:9]
6
10

FIG. 12

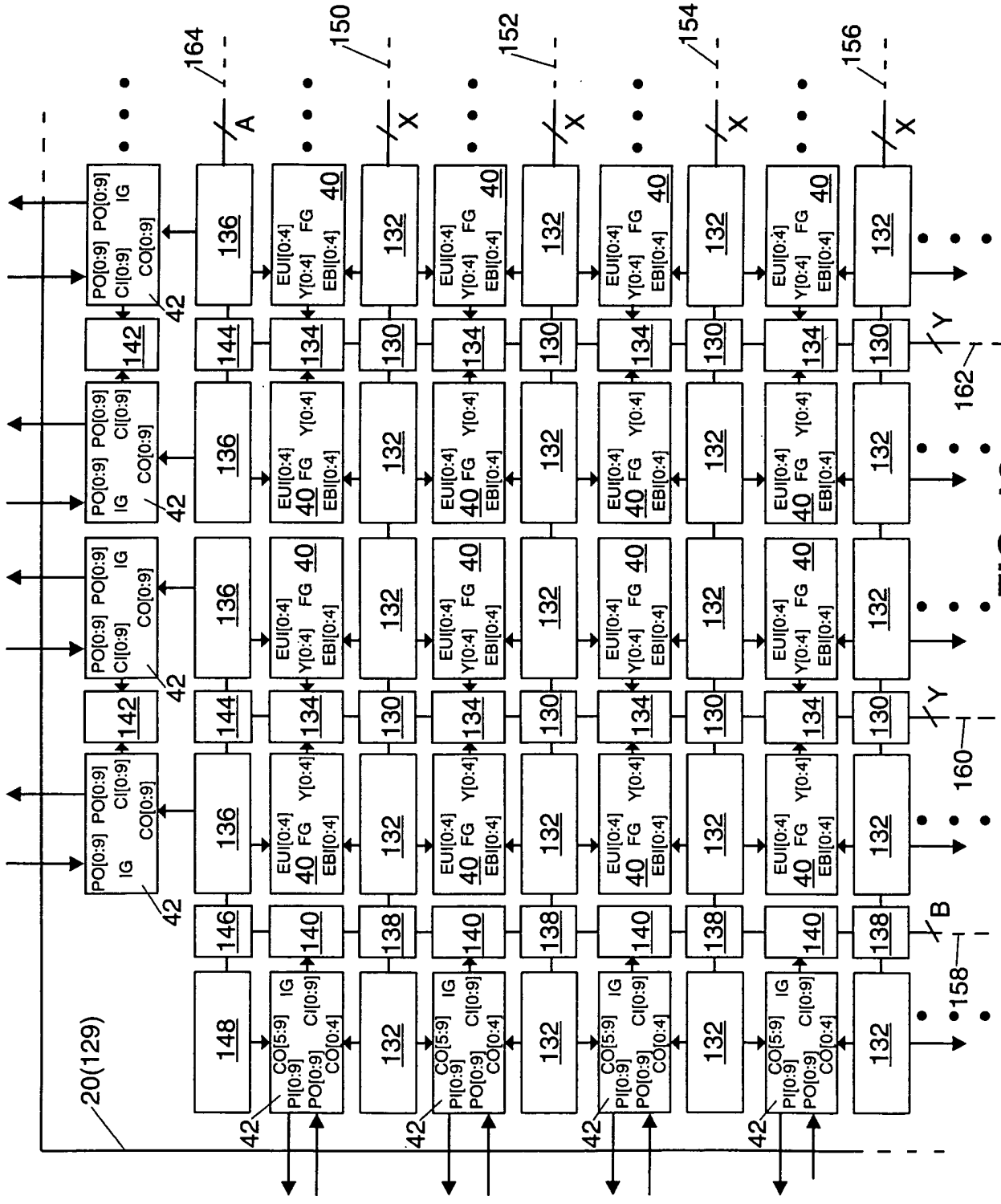
20(129)
42
148
146
140
138
132
136
144
142
134
130
164
150
152
154
156
A
X
Y
B
158
160
162
PO[0:9] PO[0:9] IG
CI[0:9] CO[0:9]
EUI[0:4] FG
Y[0:4]
EBI[0:4]
40
CO[5:9] IG
PI[0:9] CI[0:9]
PO[0:9] CO[0:4]

FIG. 13

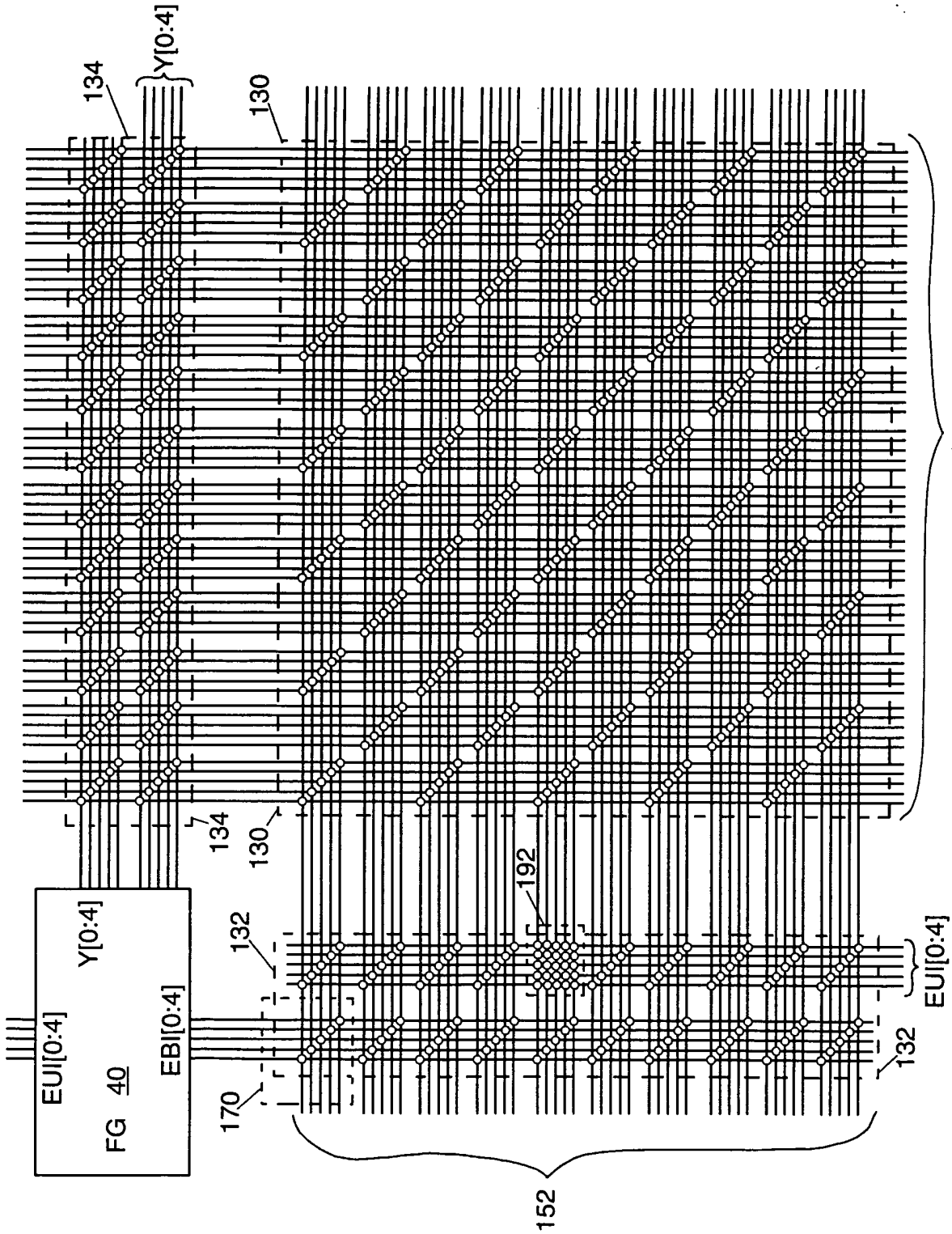
134
Y[0:4]
130
160
134
130
192
132
Y[0:4]
EUI[0:4]
EBI[0:4]
FG 40
EUI[0:4]
132
170
152

FIG.14

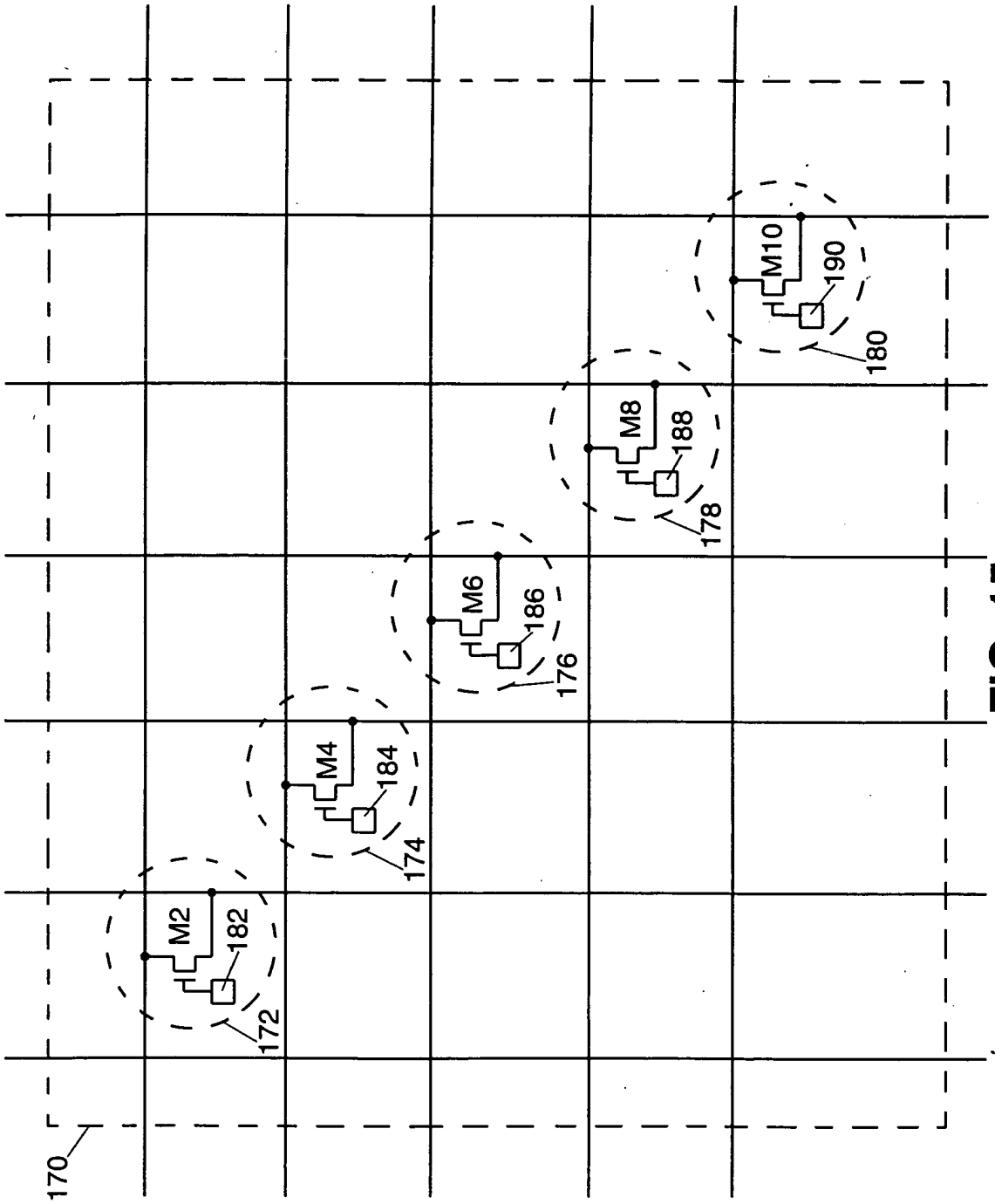

FIG. 15

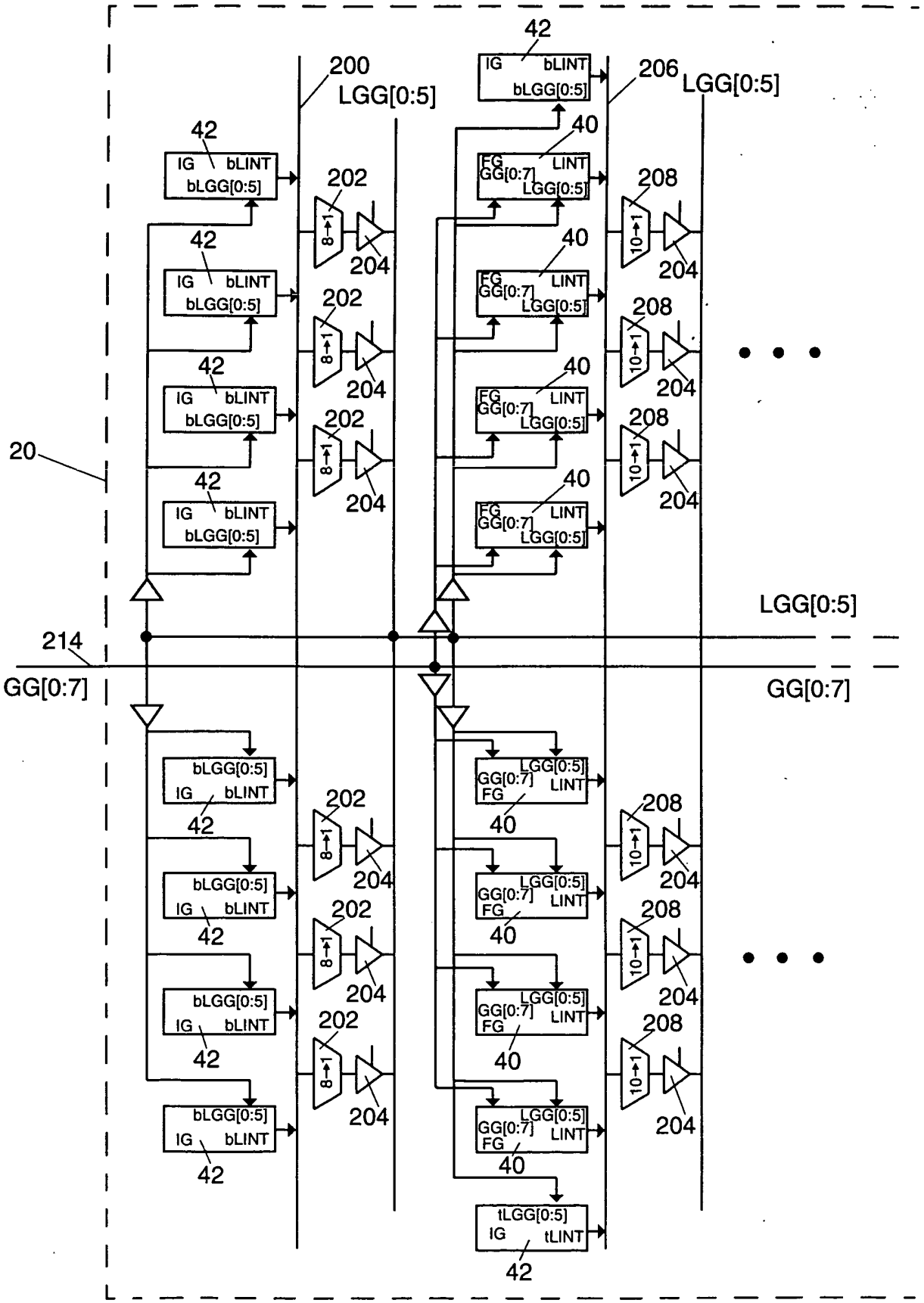
20
200
LGG[0:5]
206
LGG[0:5]
214
GG[0:7]
LGG[0:5]
GG[0:7]
42
IG
bLINT
bLGG[0:5]
40
FG
GG[0:7]
LINT
LGG[0:5]
202
8→1
204
208
10→1
tLGG[0:5]
tLINT

FIG. 16A

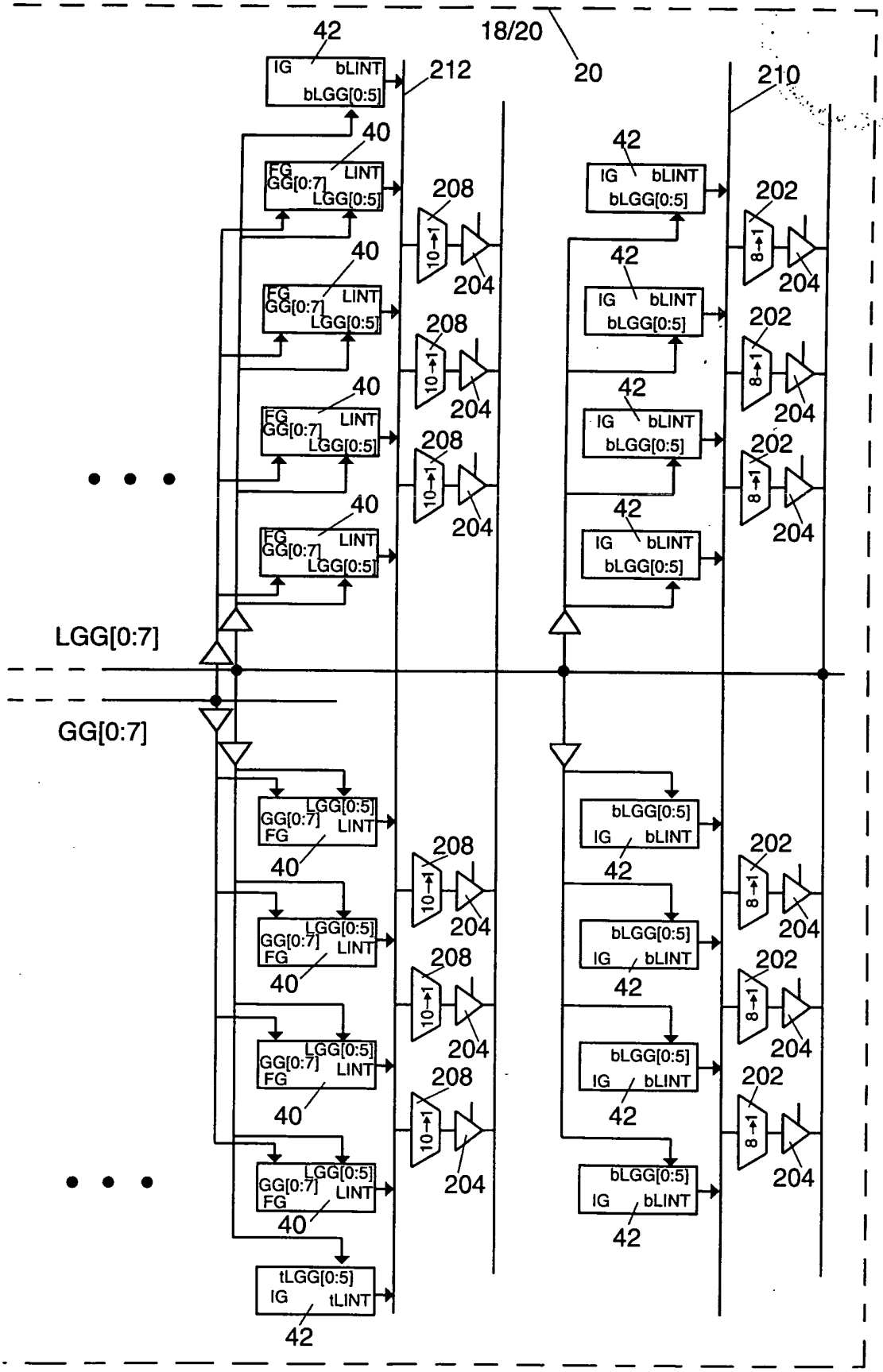
18/20
20
42
IG
bLINT
bLGG[0:5]
212
210
40
FG
GG[0:7]
LINT
LGG[0:5]
208
202
10→1
8→1
204
LGG[0:7]
GG[0:7]
tLGG[0:5]
tLINT

FIG. 16B

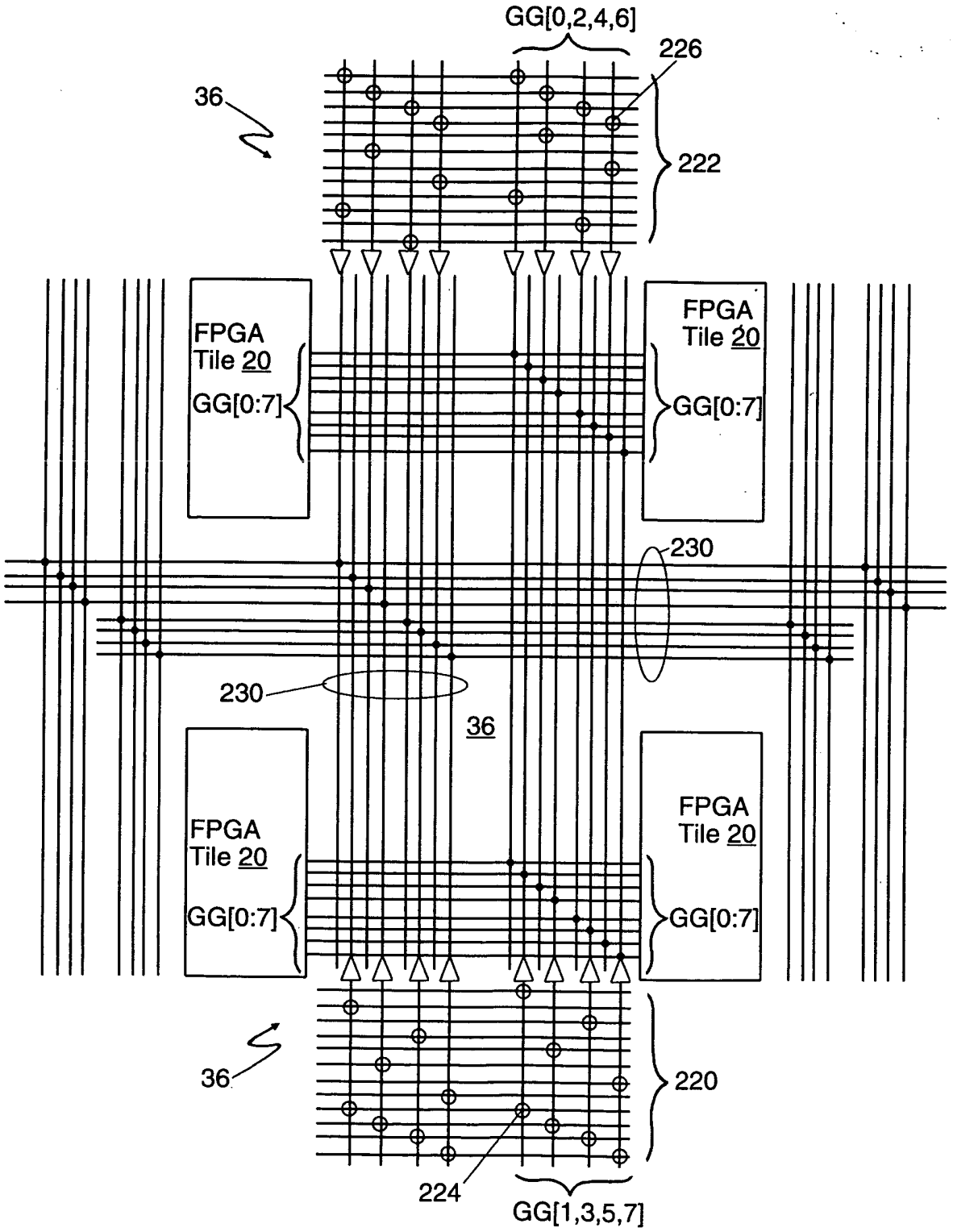
GG[0,2,4,6]
226
36
222
FPGA
Tile 20
GG[0:7]
FPGA
Tile 20
GG[0:7]
230
230
36
FPGA
Tile 20
GG[0:7]
FPGA
Tile 20
GG[0:7]
36
220
224
GG[1,3,5,7]

FIG. 17

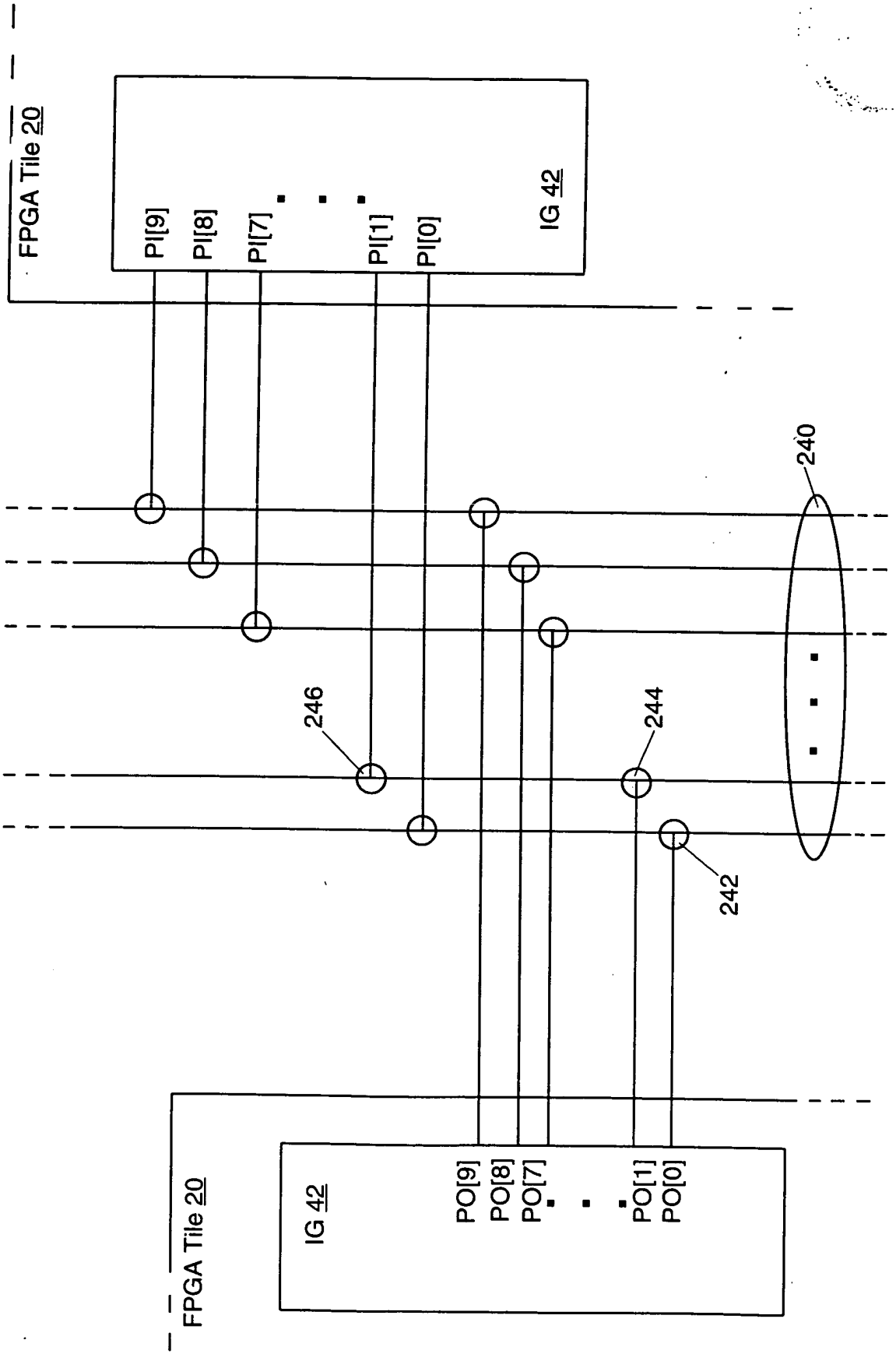
FPGA Tile 20
PI[9]
PI[8]
PI[7]
PI[1]
PI[0]
IG 42
240
246
244
242
IG 42
PO[9]
PO[8]
PO[7]
PO[1]
PO[0]
FPGA Tile 20

FIG. 18

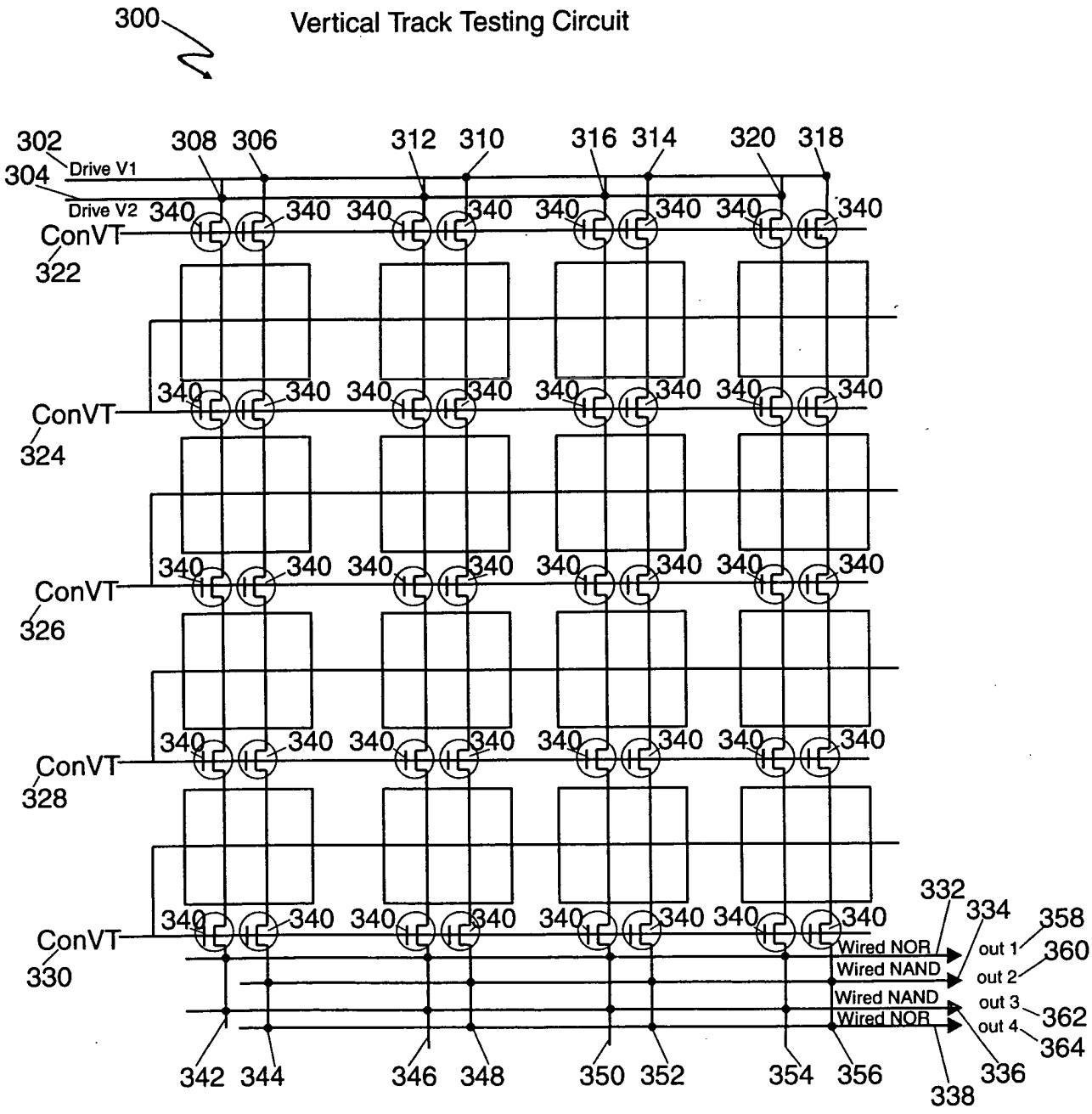
300
Vertical Track Testing Circuit
302
304
Drive V1
Drive V2
308
306
312
310
316
314
320
318
340
ConVT
322
324
326
328
330
332
334
358
360
362
364
336
338
Wired NOR
Wired NAND
Wired NAND
Wired NOR
out 1
out 2
out 3
out 4
342
344
346
348
350
352
354
356

FIG. 19

Truth Table

DriveV1	DriveV2	Out1	Out2	Out3	Out4
0	0	1	1	1	1
0	1	1	0	1	0
1	0	0	1	0	1
1	1	0	0	0	0

FIG. 20

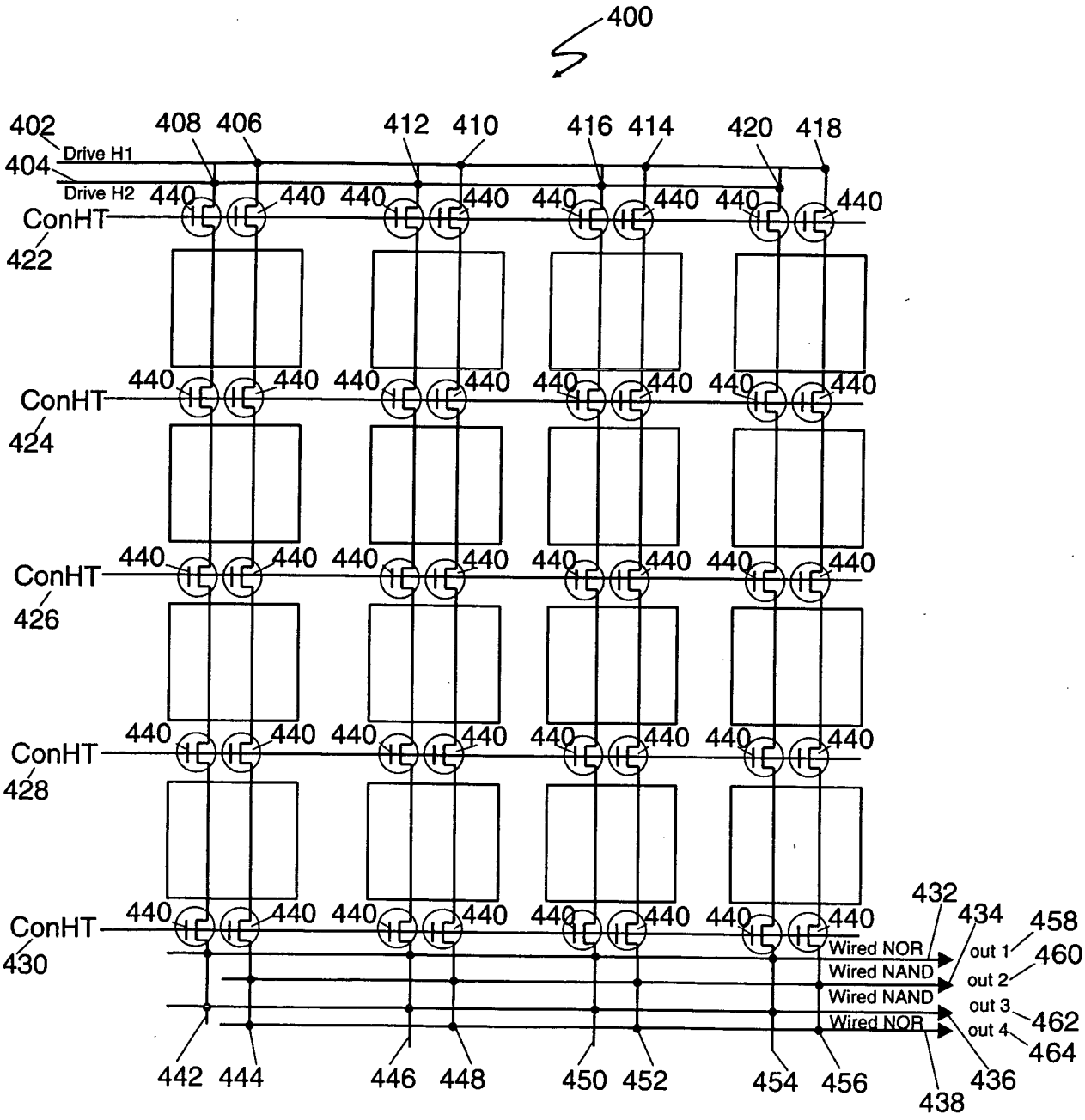
400
402
404
Drive H1
Drive H2
408
406
412
410
416
414
420
418
440
ConHT
422
424
426
428
430
Wired NOR
Wired NAND
Wired NAND
Wired NOR
out 1
out 2
out 3
out 4
432
434
458
460
462
464
436
438
442
444
446
448
450
452
454
456

FIG. 21

Truth Table

DriveH1	DriveH2	Out1	Out2	Out3	Out4
0	0	1	1	1	1
0	1	1	0	1	0
1	0	0	1	0	1
1	1	0	0	0	0

FIG. 22